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10/625,902	07/24/2003	Hideyuki Otake	OKI.556	1200

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EXAMINER	
JEANGLAUDE, JEAN BRUNER	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,902	OTAKE, HIDEYUKI	
	Examiner	Art Unit	
	Jean B. Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 7-31-06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-8,10,12-15,17 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-8,10,12-15,17,19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response To Amendments/Arguments

1. Applicant's arguments filed on August 10, 2006 have been fully considered but they are not persuasive.

2. Regarding the applicant's argument on page 8 , 2nd paragraph, the examiner acknowledges in column 3, lines 3 – 6 that Brunolli et al's reference discloses that "an embodiment of the digital potentiometer may be fabricated on an integrated circuit die using complimentary metal oxide (CMOS) transistors for the switches". However, Brunolli et al. does also give one ordinary skill in the art another choice of the embodiment of the digital potentiometer in column 4, lines 45 – 51 which reads as "N-channel and P-channel metal oxide semiconductor (NMOS and PMOS), complementary metal oxide semiconductor (CMOS), bipolar transistor, junction field effect transistor (JFET), insulated gate field effect transistor (IGFET) and the like, may be used to implement the switches and other circuits according to the embodiments of the present invention." As noted in this quotation, an artisan in the art would also have a choice of using N-channel and P-channel transistors as switches the same way "complimentary metal oxide (CMOS) transistors for the switches" may be used. Therefore, the argument is moot.

3. Regarding the applicant's argument on page 8, 3rd paragraph that "S1 through S4 in fig. 3 of Brunolli et al.'s reference cannot be interpreted as the second switching circuit".

4. The Examiner respectfully disagrees. Brunolli et al. discloses in fig. 3 a digital switched potentiometer in which three different set of switches are used: first, second

and third switch elements. Switches S1-S4 can be used as second switch element to perform the same function as the claimed invention. Therefore, the argument is moot.

5. For at least these reasons, the rejection is maintained as follows:

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3, 5 – 6, 8, 10, 12, 13, 15, 17, 19, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Brunolli et al. (US Patent Number 6,201,491).

8. Regarding claim 1, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) comprising: a first potential terminal (V_{CC}) for supplying a first potential; a second potential terminal (the ground) for supplying a second potential; an output node (output) for outputting an analog signal (figs. 3, 5) ; a first resistor circuit (302, fig. 3; 902, fig. 5) having a plurality of first resistors connected in series between a first node and the output node through a plurality of first connecting points (figs. 3, 5); a first switching circuit (S9,...S12) including P-channel type MOS transistors each of the P-channel type MOS transistor connected directly to the first potential terminal (V_{CC}) , and to respective ones of the first connecting points and the first node wherein only the P-channel type MOS transistors are connected to the first resistors as switches (figs. 3, 5) [col. 4, lines 45 – 51]; a second resistor circuit (306, fig. 3; 906, fig. 5) having a plurality of second resistors connected in series between a second node and the output node

through a plurality of second connecting points (figs. 3, 5); a second switching circuit (S1,...,S4) including N-channel type MOS transistors each of the N-channel type MOS transistors connected directly to the second potential terminal (the ground), and to respective ones of the second connecting points and the second node wherein only the N-channel type MOS transistors are connected to the second resistors as witches (figs. 3, 5) [col. 4, lines 45 – 51]; and a control circuit (col. 6, lines 6 – 16) connected to the first and second switching circuits for controlling P-channel type MOS transistors and the N-channel type MOS transistors [col. 4, lines 45 – 51].

9. Regarding claim 3, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) wherein the second switching circuit (S1,...,S4) further has a an N-channel type MOS transistor connected between the second potential terminal and the output node (figs. 3, 5) [col. 4, lines 45 – 51].

10. Regarding claim 5, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) wherein the control circuit includes a first decoder for controlling the P-channel type MOS transistors [the first switches] [col. 4, lines 45 – 51] and a second decoder for controlling the N-channel type MOS transistors [the second switches] [col. 4, lines 45 – 51] (col. 6, lines 6 – 16).

11. Regarding claim 6, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) , wherein the first potential is a reference potential (Vcc =Vref) and the second potential is a ground potential (ground) (col. 6, lines 17, 18).

12. Regarding claim 8, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) comprising: a first potential terminal (V_{CC}) supplying a first potential; a second

potential terminal (the ground) supplying a second potential; an output node (the output) providing an analog signal; a plurality of first resistors (302, fig. 3; 902, fig. 5) connected in series between a first node and the output node, the first resistors being connected to each other at a plurality of first connecting points (figs. 3, 5); a plurality *of* first switches (S9,...S12) each of which is connected directly to the first potential terminal (Vcc), and to respective ones of the first connecting points and the first node, wherein only P-channel type MOS transistors are connected to the first resistors as switches (figs. 3, 5) [col. 4, lines 45 – 51]; a plurality of second resistors (306, fig. 3; 906, fig. 5) connected in series between a second node and the output node, the second resistors being connected to each other at a plurality of second connecting points (figs. 3, 5); a plurality of second switches (S1,..,S4) each of which is connected directly to the second potential terminal (the ground), and to respective one of the second connecting points and the second node wherein only N-channel type MOS transistors are connected to the second resistors as switches (figs. 3, 5) [col. 4, lines 45 – 51]; and a control circuit connected to control the P-channel type MOS transistors and the N-channel type MOS transistors (col. 6, lines 6 – 16) [col. 4, lines 45 – 51].

13. Regarding claim 10, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5), further comprising an additional N-channel type MOS transistor (S1,..., S4) connected between the second potential terminal and the output node (figs. 3, 5) [col. 4, lines 45 – 51].

14. Regarding claim 12, Brunolli et al. discloses a digital--to-analog converting circuit wherein the control circuit includes a first decoder for controlling the P-channel type

MOS transistor and a second decoder for controlling the N-channel type MOS transistors (col. 6, lines 6 – 16) [col. 4, lines 45 – 51].

15. Regarding claim 13, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) , wherein the first potential is a reference potential (Vcc=Vref) and the second potential is a ground potential [ground] (col. 6, lines 17, 18).

16. Regarding claim 15, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) comprising: a first potential terminal (Vcc) supplying a first potential; a second potential terminal (ground) supplying a second potential; an analog node providing an analog signal (the node at the output); a plurality of first resistors (302, fig. 3; 902, fig. 5) connected in series between a first node and the analog node through a plurality of first connecting nodes (figs. 3, 5); a plurality of P-channel type MOS transistors (S9,...S12) each of which is connected directly to the first potential terminal, and to respective ones of the first connecting nodes and the first node (figs. 3, 5) [col. 4, lines 45 – 51]; a plurality of second resistors (306, fig. 3; 906, fig. 5) connected in series between a second node and the output node through a plurality of second connecting nodes (figs. 3, 5); a plurality of N-channel type MOS transistors (S1,...,S4) each of which is connected directly to_the second potential terminal, and to respective ones_of the second connecting nodes and the second node (figs. 3, 5) [col. 4, lines 45 – 51]; and a control circuit connected to control the P-channel type MOS transistors and the N-channel type MOS transistors (col. 6, lines 6 – 16) [col. 4, lines 45 – 51].

17. Regarding claim 17, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) further comprising an additional N-channel type MOS transistors (S1,...,S4)

connected between the second potential terminal and the output node (figs. 3, 5) [col. 4, lines 45 – 51].

18. Regarding claim 19, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5), wherein the control circuit includes a first decoder for controlling P-channel type MOS transistors and a second decoder for controlling the N-channel type MOS transistors (col. 6, lines 6 – 16).

19. Regarding claim 20, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5), wherein the first potential is a reference potential (Vcc=Vref) and the second potential is a ground potential (col. 6, lines 17, 18).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 7, 14, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brunolli et al. (US Patent Number 6,201,491) in view Leung et al. (US Patent Number 6,400,300).

22. Regarding claims 7, 14, 21, Brunolli et al. discloses all the limitations as discussed above except the digital-to-analog converting circuit comprising an amplifier connected to the output node for amplifying analog signal. However, Leung et al., in a related field, discloses a DAC (figs. 1) comprising an amplifier (26) connected to the output node for amplifying analog signal (fig. 1). Therefore, it would have been obvious

to one of ordinary skill in the art at the time the invention was made to modify Brunolli et al.'s system with that of Leung et al. in order to carry out conversion process.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jean Bruner Jeanglaude

Jean Bruner Jeanglaude
Primary Examiner
September 12, 2006